Asterfusion 400G QSFP-DD DR4 MPO-12 APC SMF 500m Optical Transceiver

Features

- 8x53.125Gb/s PAM4 electrical interface (400GAUI-8)
- 4x106.25Gb/s PAM4 optical architecture
- Maximum 500m SMF with FEC
- Power consumption < 8W
- Hot Pluggable QSFP56-DD form factor
- MPO-12 APC connector receptacle
- I2C interface is supported to read and control the status of this product
- Built-in digital diagnostic functions
- Compliant with CMIS
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- Class 1 laser safety
- RoHS compliant

Overview

The Asterfusion QSFP-DD 400G DR4 optical transceiver module is designed for 400 Gigabit Ethernet applications. It converts 8 channels of 53.125Gb/s PAM4 electrical input data to 4 parallel channels of 106.25Gb/s optical signals for 425Gb/s optical transmission. Reversely, on the receiver side, the module converts 4 channels of 106.25Gb/s optical signals to 8 channels of 53.125Gb/s (PAM4) electrical output data. This module supports data transmission distances up to 500m over SMF with Forward Error Correction (FEC).

The form factor of OT-400G-QDD-DR4 is QSFP56-DD Type 2A and the optical interface uses MPO-12 APC connectors. It supports digital diagnostic functions and is fully compatible with the Common Management

Interface Specification (CMIS) and QSFP-DD MSA, IEEE 802.3bs 400GBASE-DR4 protocol, and 400GAUI-8 standard.

Product Applications

- AI Training Fabric
- AI Inference Fabric
- Data Center Fabric
- Ethernet Storage Fabric
- HPC (High Performance Computing)
- Supercomputer
- Telecom Backbone

Block Diagram

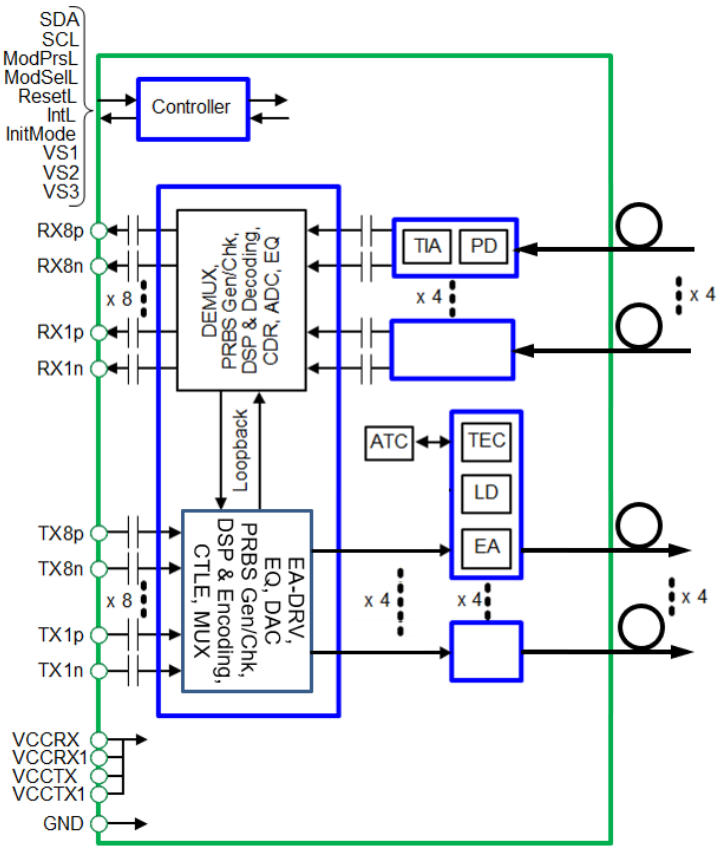

Figure 1 The 400G QSFP-DD DR4 Optical Transceiver Block Diagram

Networking

This product is allowed for two typical applications: The first application is QSFP-DD DR4 to QSFP-DD DR4 point to point communication.

Figure 2 Connect two 400G-port switches

The second application is QSFP-DD DR4 to 4 x QSFP28 DR1 breakout communication.

Figure 3 Connect 1 x 400G-port switch to 4 x 100G-port switches

Specifications

Electrical Specifications

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				8	W	
Supply Current	Icc			3.2	A	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Data Rate Accuracy		-100		100	ppm	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	PAM4
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	
Differential Termination Mismatch	TP1			10	%	

Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	[2]
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	[2]
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	
Receiver (each Lane) [1]						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	PAM4
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4	0.265			UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4	0.2			UI	
Far-end Eye Height, Differential	TP4	30			mV	

Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	

Notes:

1. Electrical receiver output is squelched for loss of optical input signal.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Transmitter						
Signaling rate, each lane		26.5625± 100ppm			Gbd	PAM4
Center Wavelength	**λ**C	1304.5		1317.5	nm	
Side-mode suppression ratio	**SMSR**	30			dB	
Average Launch Power, each Lane	P_{AVG}	-2.9		4.0	dBm	[1]
Outer Optical Modulation Amplitude (OMAouter), each Lane	P_{OMA}	-0.8		4.2	dBm	[2]
Launch power in OMA minus TDECQ, each lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	
RIN21 OMA				-136	dB/Hz	
Optical Return Loss Tolerance	TOL			21.4	dB	

Average Launch Power OFF Transmitter, each Lane	Poff			-15	dBm	
Transmitter reflectance	TR			-26	dB	[3]
Receiver						
Signaling rate, each lane		26.5625± 100ppm	Gbd	PAM4		
Center Wavelength	λC	1304.5		1317.5	nm	
Average Receive Power, each Lane	Pin	-5.9		4	dBm	[4]
Receive Power (OMA_{outer}), each Lane				4.2	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN	Max (-3.9, SECQ -5.3)			dBm	[5] [6]
Receiver Reflectance	RR			-26	dB	
Stressed receiver sensitivity (OMAouter), each lane				-1.9	dBm	[5] [7]
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	3.4			dB	
OMAouter of each aggressor lane		4.2			dBm	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. For when Pre-FEC BER is 2.4 x 10-4.
6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

7. Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3-2022 124.1.1.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

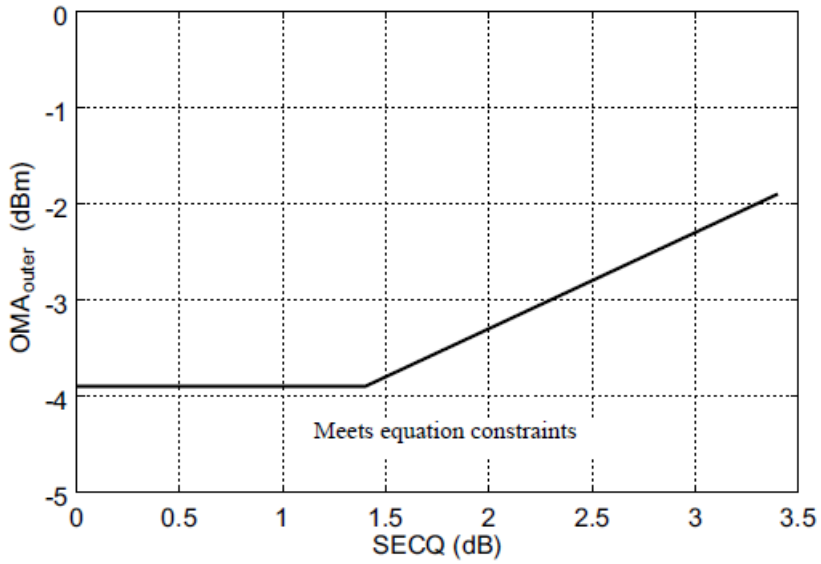

Figure 4 Illustration of Receiver Sensitivity

Optical Interface Lanes and Assignment

The optical interface port is an MPO-12 receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5.

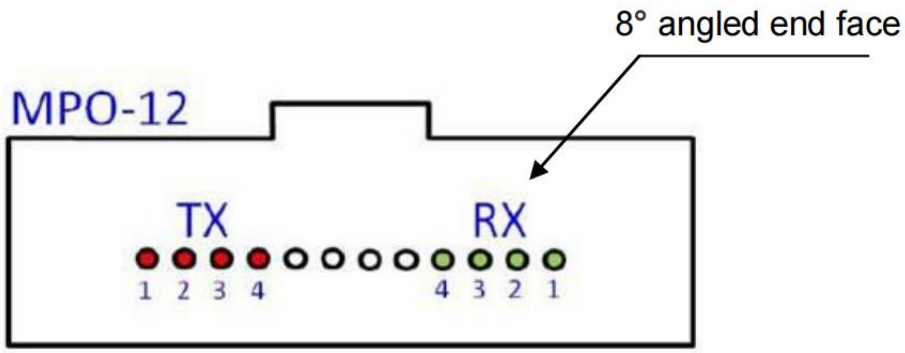

Figure 5 Optical Receptacle and Channel Orientation

Mechanical Dimensions

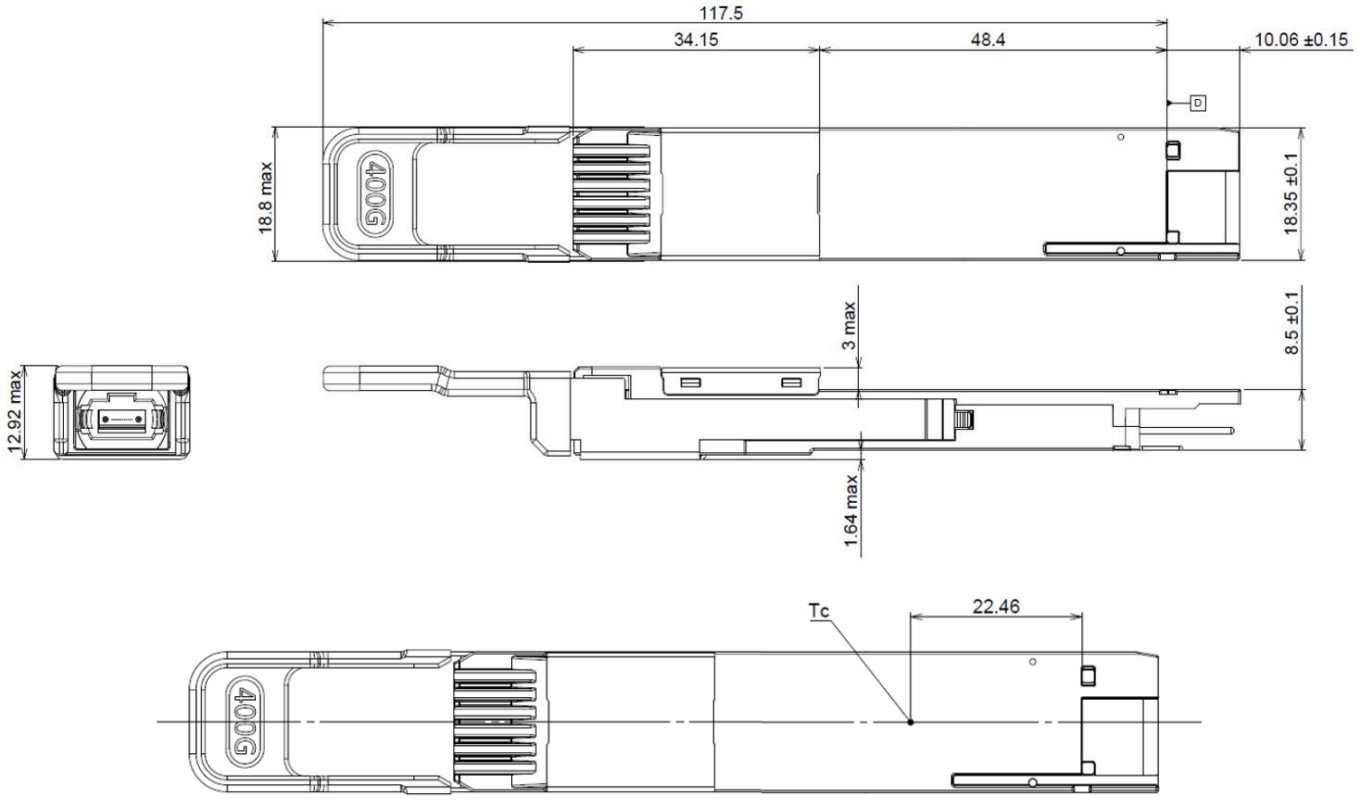

Figure 6 Mechanical Specifications (mm)

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Note
Storage Temperature	TS	-40	85	ºC	
Operating Case Temperature	TOP	0	70	ºC	
Power Supply Voltage	VCC	0	3.6	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	TOP	0		70	ºC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	

Data Rate, each Lane			26.5625		GBd	PAM4
Link Distance	D			500	m	

PIN Description

The electrical interface of QSFP56-DD module consists of 76 contacts edge connectors. It complies with the QSFP-DD MSA Specification, see http://www.qsfp-dd.com .

QSFP56-DD Pin Description

Pin #	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non- Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non- Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B

29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non- Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non- Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non- Inverted Data Input	3A

72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non- Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

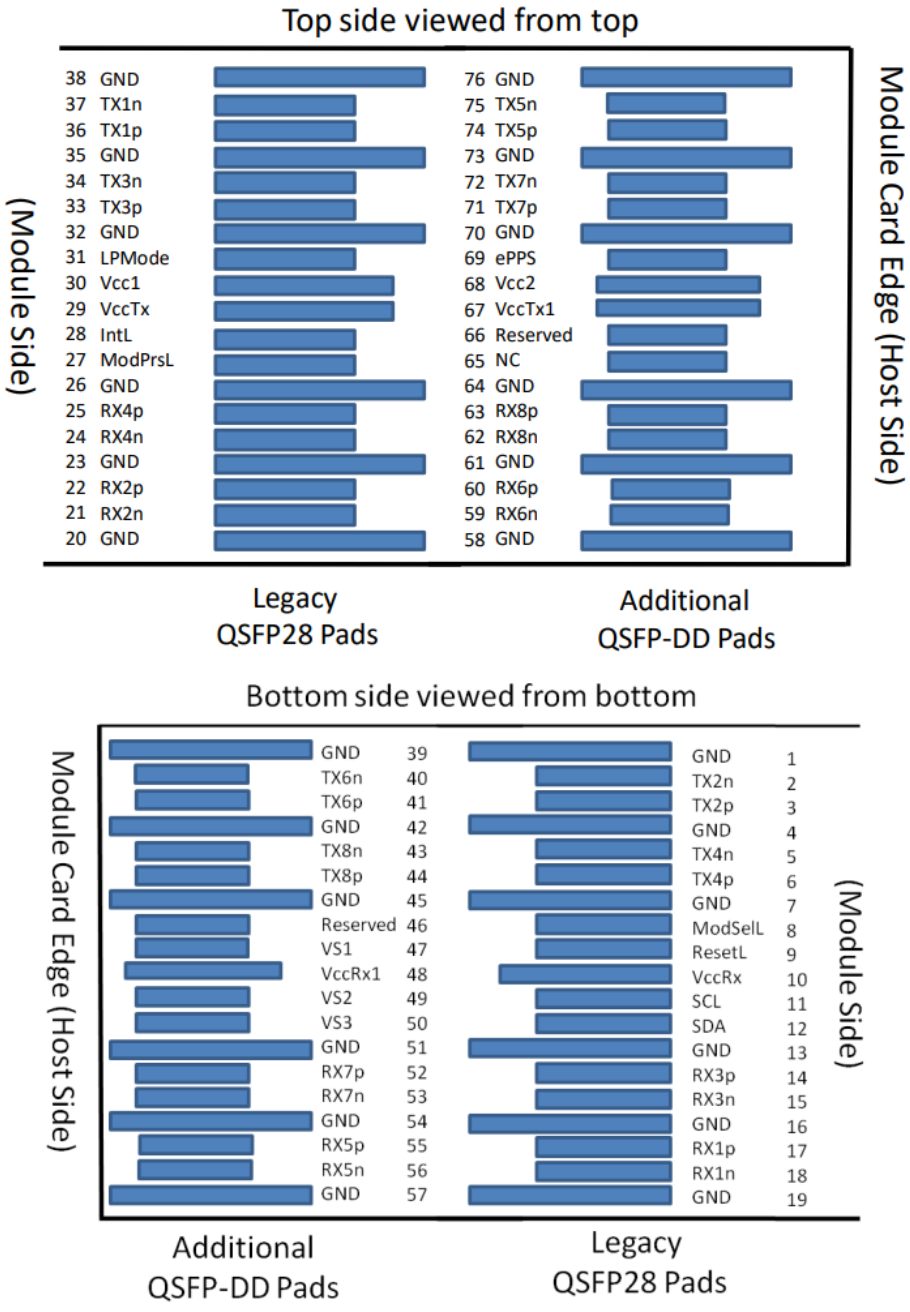

Figure 7 Electrical Pin-out Details

QSFP-DD Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Description
SCL and SDA	VOL	0	0.4	V	IOL (max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
SCL and SDA	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	ResetL shall be pulled to Vcc in the module. A low level on it for longer than t_Reset_init initiates a complete module reset.
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3 kohm pullup resistor, max. For 1000 kHz clock rate refer to [1].
	Cb		200	pF	For 400 kHz clock rate use 1.6 kohm pullup resistor, max. For 1000 kHz clock rate refer to [1].
LPMode,ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	Vcc-0.5	Vcc+0.3	V	10 kohm pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL= 2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

Note:

1. All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10kohms and less than 100pF.

Regulatory Compliance

Asterfusion OT-400G-QDD-DR4 transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC/EN 60825-1:2014 (3rd Edition) FDA 21 CFR 1040.10 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007)

Electrical Safety	EN 62368-1:2014 IEC 62368-1:2014 UL 62368-1:2014
CE EMC	EN55032:2015 EN55035:2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP-DD MSA Specification
2. CMIS

ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114- A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Order Information

Part Number	Description
OT-400G-QDD-DR4	400G, QSFP-DD, DR4, MPO12/APC, 1310nm SMF, 500m/OS2, 8W

Warranty and Service Support

Asterfusion optical transceivers come with 2-year Basic H/W service and warranty, preloaded perpetual licensed AsterNOS and 1-year AsterNOS upgrade subscription.

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