

Asterfusion 800G OSFP 2xFR4 Dual Duplex LC SMF 2km Optical Transceiver

Features

- 8 x 106.25G PAM4 electrical modulation
- 8 x 106.25G PAM4 optical modulation
- Maximum link length of 2km G.652 SMF with KP-FEC
- Power consumption <16W
- SiPh (silicon photonics) transceiver
- Hot Pluggable OSFP form factor
- Dual duplex LC receptacles
- 7nm Broadcom DSP
- 3D packaging
- Built-in digital diagnostic functions
- Compliant with CMIS V4.0
- Finned-top for air-cooled switches
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- Class 1 laser safety
- RoHS compliant (lead free)

Overview

The Asterfusion OSFP 800G 2xFR4 optical transceiver module is a low-power, high-density, pluggable OSFP module designed for 800 Gigabit Ethernet applications. The silicon photonics transceiver module adopts an advanced photonics (SiPh) platform, using SiPh chips that integrate active and passive optoelectronic components, 3D packaging, and powerful 7nm DSP chips for

unparalleled performance and efficiency. The optical module supports 8×106.25Gbps (total 850Gbps) data rates and achieves a maximum link length of 2km over G.652 standard single-mode fiber (SMF) with KP-FEC (Forward Error Correction).

The module supports single-mode fiber systems with a nominal wavelength of 1310 nm. It is compliant with OSFP MSA and IEEE 802.3 protocol. It supports digital diagnostic functions and is fully compatible with the Common Management Interface Specification (CMIS) 4.0.

Product Applications

- AI Training Fabric
- AI Inference Fabric
- Data Center Fabric
- Ethernet Storage Fabric
- HPC (High Performance Computing)
- Supercomputer
- Telecom Backbone

Block Diagram

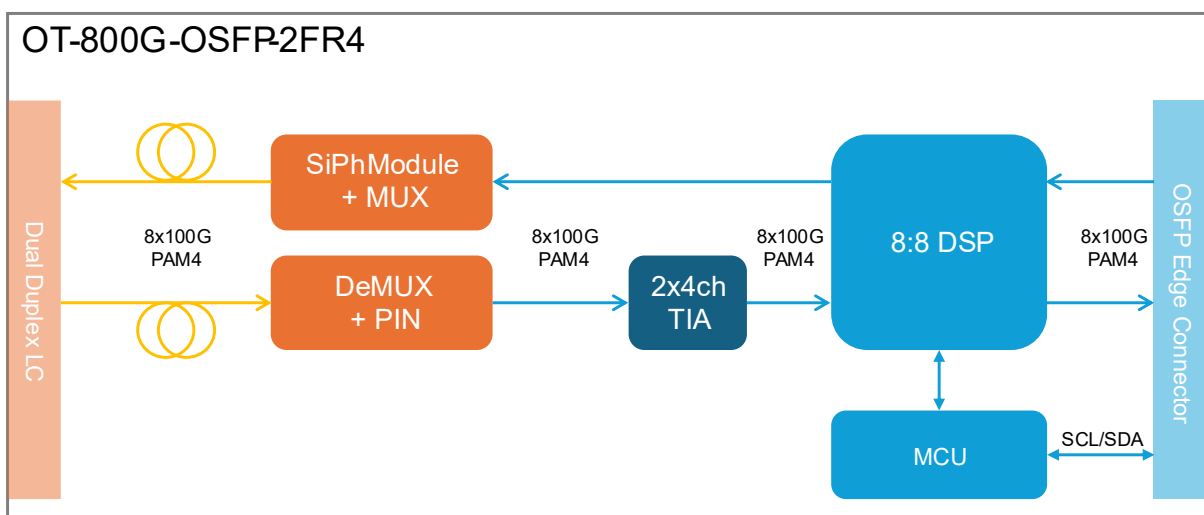


Figure 1 800G OSFP 2xFR4 Optical Transceiver Block Diagram

Networking

Connect 800G-port switches by 2 single mode fiber cable with LC Duplex connector.

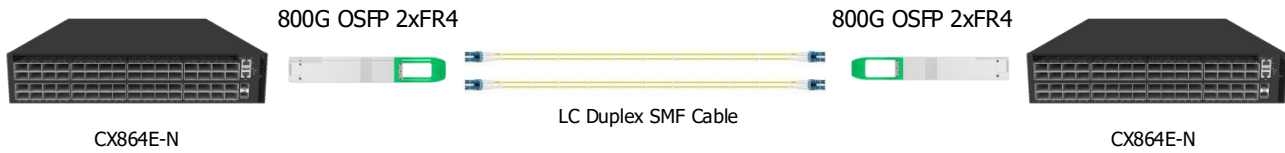


Figure 2 Connect two switches

Specifications

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Pre-FEC Bit Error Rate ^[1]	BER			2.4E-4	
Differential input impedance ^[2]	Z _{in}	90	100	110	ohm
Differential Output impedance ^[3]	Z _{out}	90	100	110	ohm
Differential input voltage amplitude	ΔV _{in}	400		900	mVp-p
Differential output voltage	ΔV _{out}			850	mVp-p
Input Logic Level High	V _{IH}	2.0		V _{CC}	V
Input Logic Level Low	V _{IL}	0		0.8	V
Output Logic Level High	V _{OH}	V _{CC} -0.5		V _{CC}	V
Output Logic Level Low	V _{OL}	0		0.4	V

Note:

1. BER=2.4E-4, tested under PRBS31Q@53.125GBd, Pre-FEC.
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Centre Wavelength	L1	1264.5		1277.5	nm
Centre Wavelength	L2	1284.5		1297.5	nm
Centre Wavelength	L3	1304.5		1317.5	nm
Centre Wavelength	L4	1324.5		1337.5	nm
Centre Wavelength	L5	1264.5		1277.5	nm
Centre Wavelength	L6	1284.5		1297.5	nm
Centre Wavelength	L7	1304.5		1317.5	nm
Centre Wavelength	L8	1324.5		1337.5	nm
SMSR	SMSR	30			nm
Average Launch Power (each lane)	P_{out}	-3.2	-	4.4	dBm
Average Launch Power(total)	P_{total}			10.4	dBm
Optical Modulation Amplitude (OMA _{outer}), each lane	OMA _{out}	-0.2		3.7	dBm
Transmitter and dispersion eye closure for PAM4(TDECQ), each lane	TDECQ			3.4	dB
Outer Extinction Ratio	ER	3.5	-	-	dB
Average launch power of OFF transmitter, each lane	P_{off}			-16	dB
Optical Return Loss Tolerance	ORLT			17.1	dB
Receiver					
Centre Wavelength	L1	1264.5		1277.5	nm
Centre Wavelength	L2	1284.5		1297.5	nm
Centre Wavelength	L3	1304.5		1317.5	nm
Centre Wavelength	L4	1324.5		1337.5	nm
Centre Wavelength	L5	1264.5		1277.5	nm
Centre Wavelength	L6	1284.5		1297.5	nm
Centre Wavelength	L7	1304.5		1317.5	nm
Centre Wavelength	L8	1324.5		1337.5	nm
Damage threshold	R _{dam}	5.4			dBm

Average Receive power, each lane ^[2]	Pin	-7.2		4.4	dBm
Receiver Power (OMA _{outer}), each lane	OMA _{out}			3.7	dBm
Receiver Sensitivity (OMA _{outer}), each lane ^[1]	Sen			-4.6	dBm
Stressed Receiver Sensitivity (OMA _{outer}), each lane	Sen,s			-2.6	dBm
Receiver Reflectance	Pref			-26	dB
Difference in receive power between any two lanes (OMA _{outer})	D _{OMA}			4.1	dB

Note:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Optical Interface Lanes and Assignment

The optical interface port is Dual Duplex LC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 3.

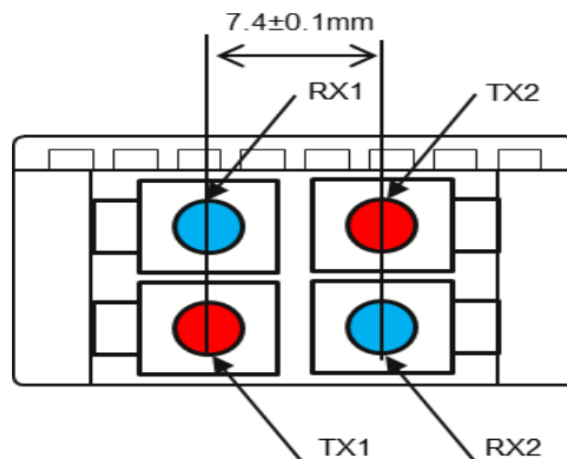


Figure 3 Optical Receptacle and Channel Orientation

Mechanical Dimensions

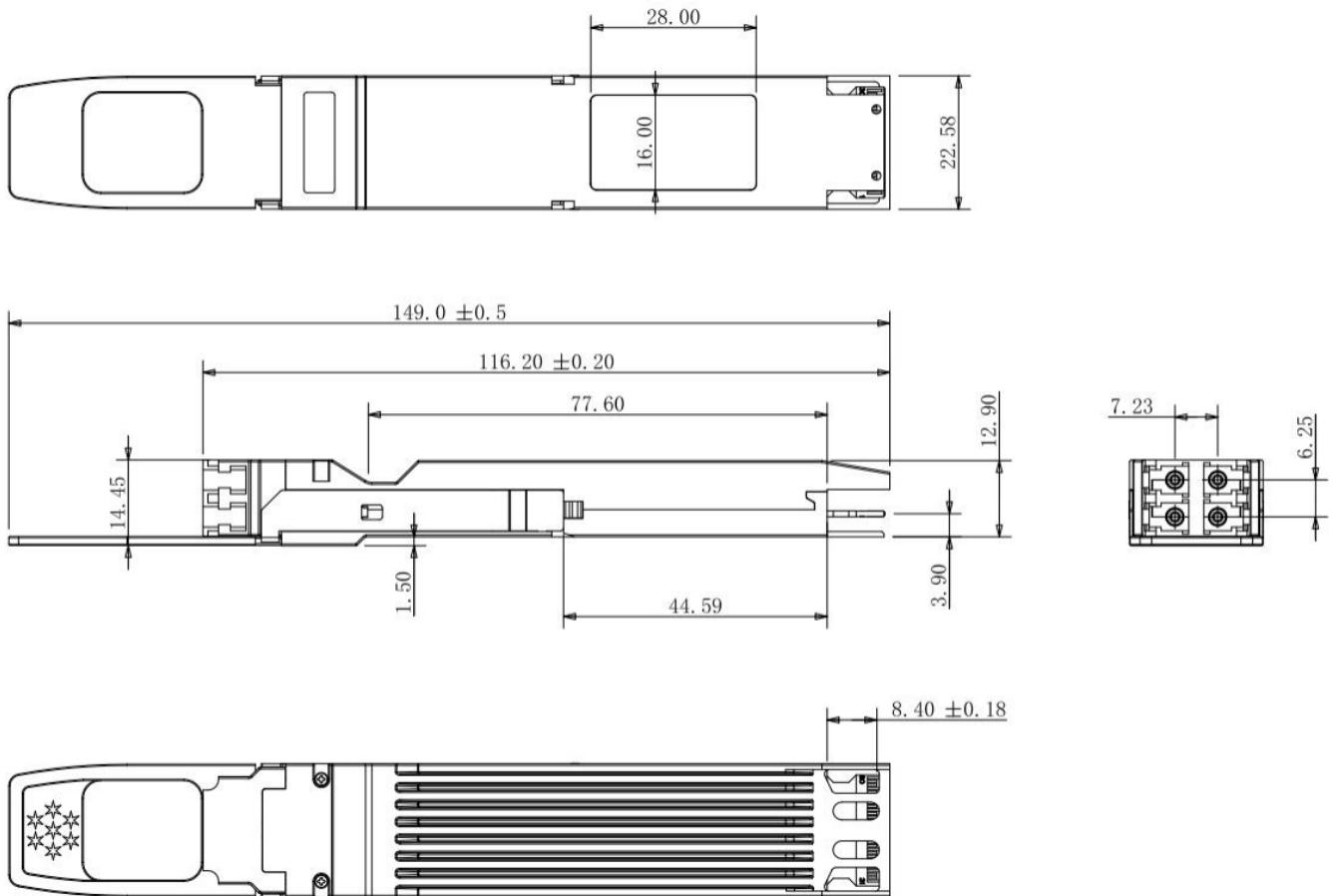


Figure 4 Mechanical Specifications (mm)

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C



Data Rate Per Lane	fd		106.25		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			16	W

PIN Description

The optical transceiver complies with the OSFP MSA Specification, see www.osfpmsa.org .

OSFP Pin Description

Pin	Symbol	Description	Logic	Direction
1	GND	Ground		
2	TX2p	Transmitter Data Non- Inverted	CML-I	Input from Host
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host
4	GND	Ground		
5	TX4p	Transmitter Data Non- Inverted	CML-I	Input from Host
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host
7	GND	Ground		
8	TX6p	Transmitter Data Non- Inverted	CML-I	Input from Host
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host
10	GND	Ground		
11	TX8p	Transmitter Data Non- Inverted	CML-I	Input from Host
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	Bi- directional
15	VCC	+3.3V Power		Power from Host
16	VCC	+3.3V Power		Power from Host
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi- directional
18	GND	Ground		



19	RX7n	Receiver Data Inverted	CML-O	Output to Host
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host
21	GND	Ground		
22	RX5n	Receiver Data Inverted	CML-O	Output to Host
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host
24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O	Output to Host
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host
27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O	Output to Host
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host
33	RX2n	Receiver Data Inverted	CML-O	Output to Host
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host
36	RX4n	Receiver Data Inverted	CML-O	Output to Host
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host
39	RX6n	Receiver Data Inverted	CML-O	Output to Host
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host
42	RX8n	Receiver Data Inverted	CML-O	Output to Host
43	GND	Ground		
44	INT/ RSTn	Module Interrupt / Module Reset	Multi-Level	Bi- directional
45	VCC	+3.3V Power		Power from Host
46	VCC	+3.3V Power		Power from Host
47	SDA	2-wire Serial interface data	LVC MOS-I/O	Bi- directional
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	Input
50	TX7p	Transmitter Data Non- Inverted	CML-I	Input from Host
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host
53	TX5p	Transmitter Data Non- Inverted	CML-I	Input from Host
54	GND	Ground		
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host

56	TX3p	Transmitter Data Non- Inverted	CML-I	Input from Host
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host
59	TX1p	Transmitter Data Non- Inverted	CML-I	Input from Host
60	GND	Ground		

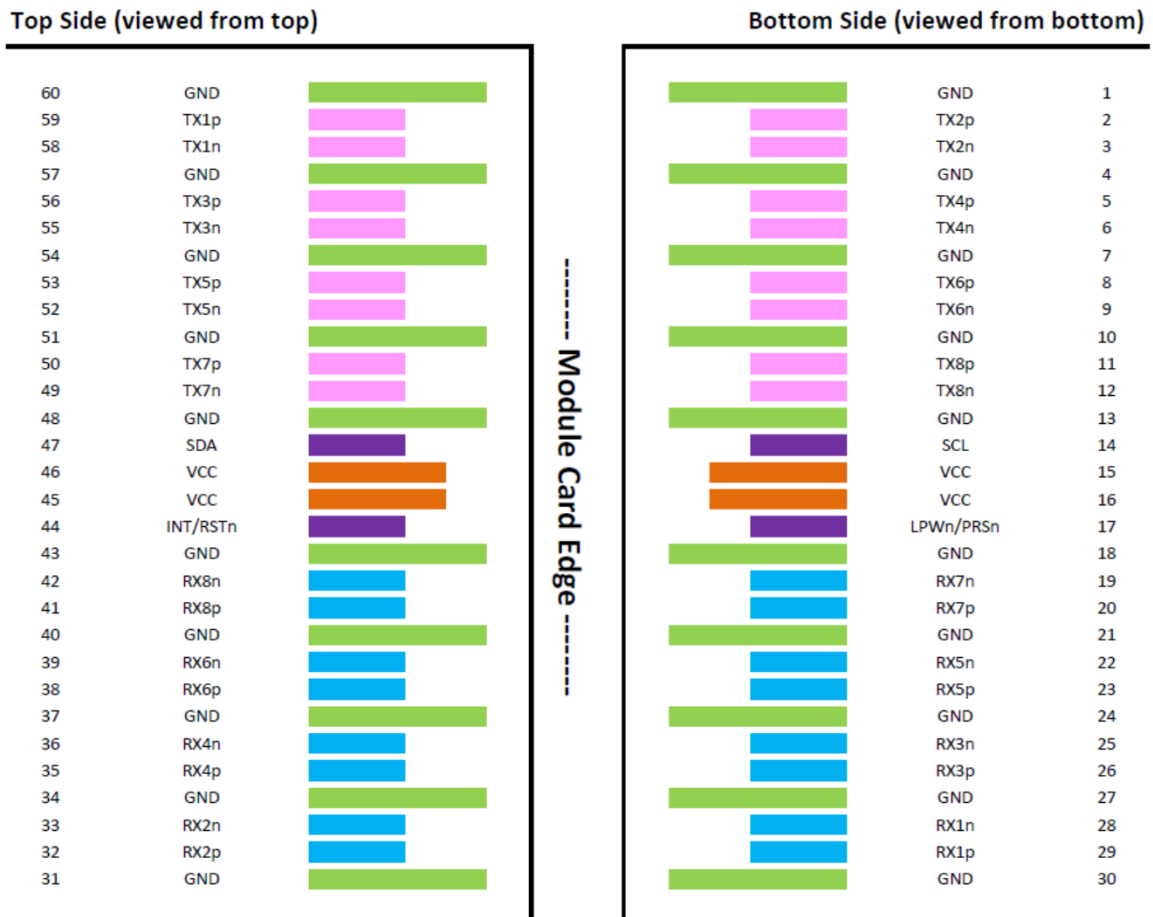


Figure 5 Electrical Pin-out Details

OSFP Control Signals

Name	Function	Description
LPWn/PRSn	Input/output	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.
INT/RSTn	Input/output	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal



		requires the circuit as described in the OSFP Specification.
SCL	Bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	°C	Over operating temp
Supply voltage monitor absolute error	DMI_VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2		+2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2		+2	dB	Per channel

Regulatory Compliance

Asterfusion OT-800G-OSFP-2FR4 transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3 rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1:2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863

CE EMC	EN55032:2015 EN55035:2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. OSFP MSA
2. CMIS V4.0
3. IEEE 802.3
4. OIF CEI-112G-VSR

Order Information

Part Number	Description
OT-800G-OSFP-2FR4	800G, OSFP, 2FR4, Dual Duplex LC, SMF, 2km

Warranty and Service Support

Asterfusion optical transceivers come with 2-year Basic H/W service and warranty.

To acquire more info about company, products, and solutions: www.cloudswit.ch
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