Asterfusion 800G QSFP-DD 2DR4 Dual MPO-12 APC SMF 500m Optical Transceiver

Features

- 8 x 106.25G PAM4 electrical modulation
- 8 x 106.25G PAM4 optical modulation
- Maximum 500m on SMF
- Power consumption <16.5W
- Hot Pluggable QSFP-DD form factor
- Dual MPO-12 APC connector receptacle
- Internal CDR circuits on both receiver and transmitter channels
- I2C interface is supported to read and control the status of this product
- Built-in digital diagnostic functions
- Compliant with CMIS
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- Class 1 laser safety

Overview

The Asterfusion QSFP-DD 800G 2DR4 500m optical transceiver is a low-power, high-density, pluggable QSFP module designed for 800 Gigabit Ethernet applications. It integrates 8 independent 106.25Gb/s PAM4 channels for aggregated 800Gb/s bandwidth. Each lane can achieve 106.25 Gbps, supporting distances up to 500m over SMF with Forward Error Correction (FEC).

The module supports single-mode fiber systems with a nominal wavelength of 1310 nm. The optical interface uses Dual MPO-12/APC connectors. It supports digital diagnostic functions and is fully compatible with the Common Management Interface Specification (CMIS) and QSFP-DD MSA. The module is designed for integration with modern data center infrastructure, high-density network deployments, HPCs, and enterprise networks.

Product Applications

- AI Training Fabric
- AI Inference Fabric
- Data Center Fabric
- Ethernet Storage Fabric
- HPC (High Performance Computing)
- Supercomputer
- Telecom Backbone

Block Diagram

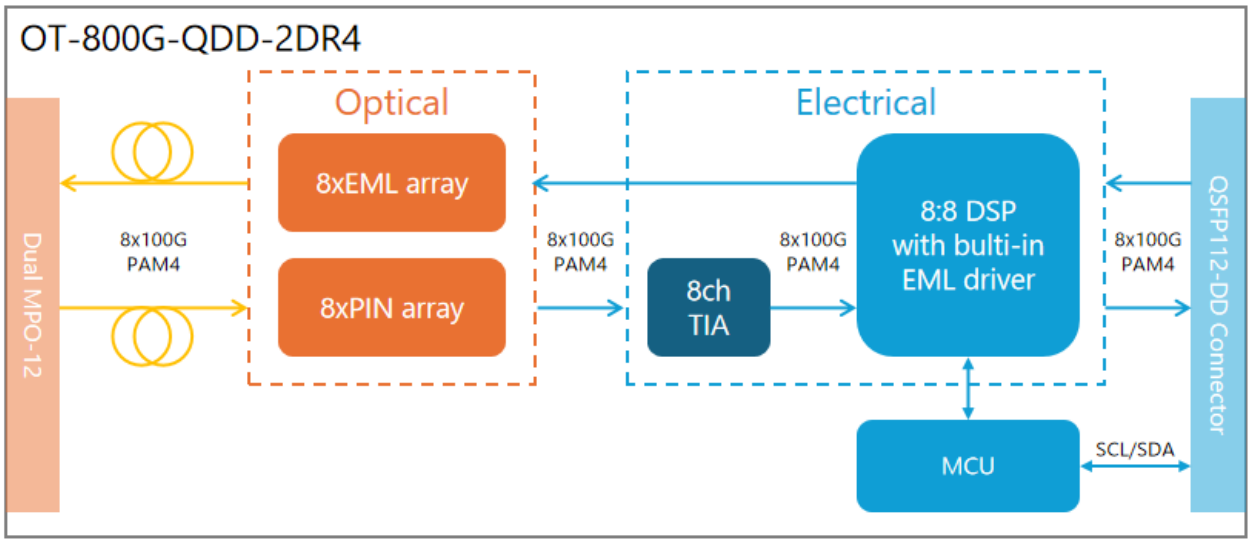

Figure 1 The 800G QSF-DD 2DR4 Optical Transceiver Block Diagram

Specifications

Electrical Specifications

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				16.5	W	
Supply Current	Icc			5	A	
Pre-FEC Bit Error Ratio (BER)				2.4E-4		
Post-FEC Bit Error Ratio (BER)				1.0E-15		
Data Rate Accuracy		-100		100	ppm	
Module input (each Lane)						
Signaling Rate, each Lane	TP1	53.125 ± 100 ppm			GBd	
Differential pk-pk voltage tolerance	TP1a	750			mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCM_{LF} High-frequency, VCM_{FB}	TP1a	 32 80			mV	
Differential-mode to	TP1	Equation			dB	
common-mode return loss, *RLcd*		(120G-2)				
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module stressed input tolerance	TP1a	See 120G.3.4.3				[1]
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode voltage tolerance	TP1	-350		2850	mV	[2]
Module output (each Lane)						

Signaling Rate, each lane	TP4	53.125			GBd	[3]
Peak-to-peak AC common-mode voltage Low-frequency, VCM_{LF} Full-band, VCM_{FB}	TP4			 32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	 mV mV	
Eye height, differential	TP4	15			mV	
Vertical eye closure	TP4			12	dB	
Common-mode to differential-mode return loss	TP4	Equation (120G-1)			dB	
Effective return loss, ERL	TP4	8.5			dB	
Differential termination mismatch	TP4			10	%	
Transition time (20% to 80%)	TP4	8.5			ps	
DC common-mode output voltage	TP4	-350		2850	mV	[2]

Notes:

1. Meets BER specified in 120G.1.1.
2. DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.
3. The signaling rate range is derived from the PMD receiver input.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Center Wavelength	λc	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	

Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	P_{AVG}	-2.9		4	dBm	[1]
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-0.8		4.2	dBm	[2]
Launch Power in OMA_{outer} minus TDECQ, each Lane for ER ≥ 5dB for ER < 5dB		-2.2 -1.9			dB	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
TDECQ – $10*\log_{10}(C_{eq})$, each Lane				3.4	dB	[3]
Extinction Ratio	ER	3.5			dB	
$RIN_{15.5}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			15.5	dB	
Transmitter Reflectance	T_R			-26	dB	[4]
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH_d	5			dBm	[5]
Average Receive Power, each Lane		-5.9		4	dBm	[6]
Receive Power (OMA_{outer}), each Lane				4.2	dBm	

Receiver Sensitivity (OMA_{outer}), each Lane	SEN			max(-3.9, *SECQ* - 5.3)	dBm	[7]
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-1.9	dBm	[8]
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-15		-9.9	dBm	
LOS De-assert	LOSD			-6.9	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity [9]						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
SECQ – $10*\log_{10}(C_{eq})$, Lane under Test				3.4	dB	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. For 100GBASE-DR, the requirement on the OMA_{outer} (min) applies even in the cases where TDECQ < 1.4dB for an extinction ratio of ≥ 5dB or where TDECQ < 1.1dB for an extinction ratio of < 5dB.
3. C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for the reference equalizer noise enhancement.
4. Transmitter reflectance is defined looking into the transmitter.
5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 5.

$$RS = \max(-3.9, SECQ - 5.3) \text{ dBm} \quad (1)$$

Where:

RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

8. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}.
9. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

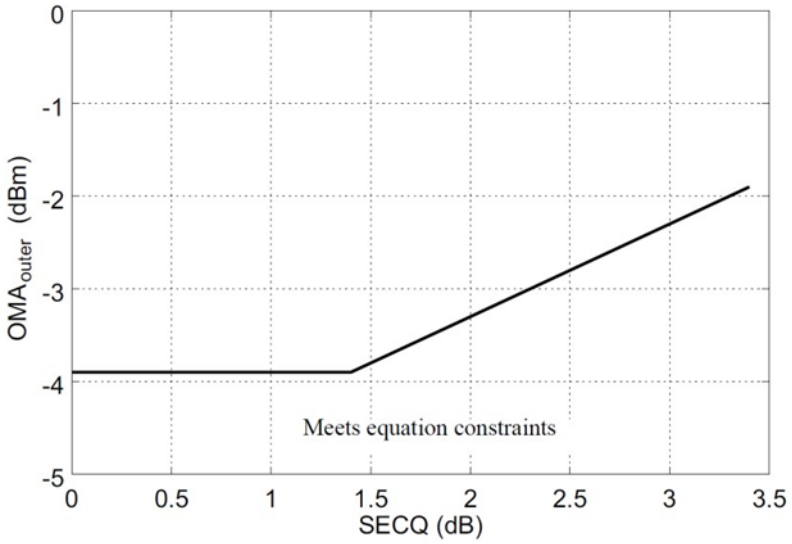

Figure 2 Illustration of Receiver Sensitivity Mask for 800G-2DR4

Optical Interface Lanes and Assignment

The optical interface port is a Dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 6.

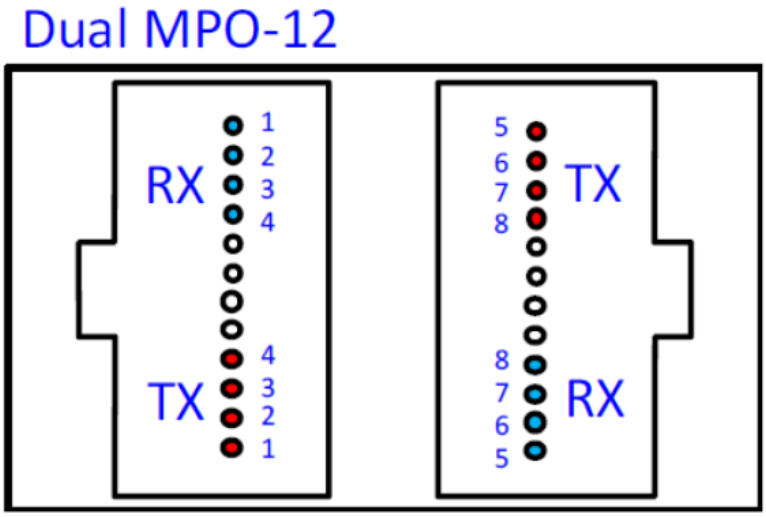

Figure 3 Optical Receptacle and Channel Orientation

Mechanical Dimensions

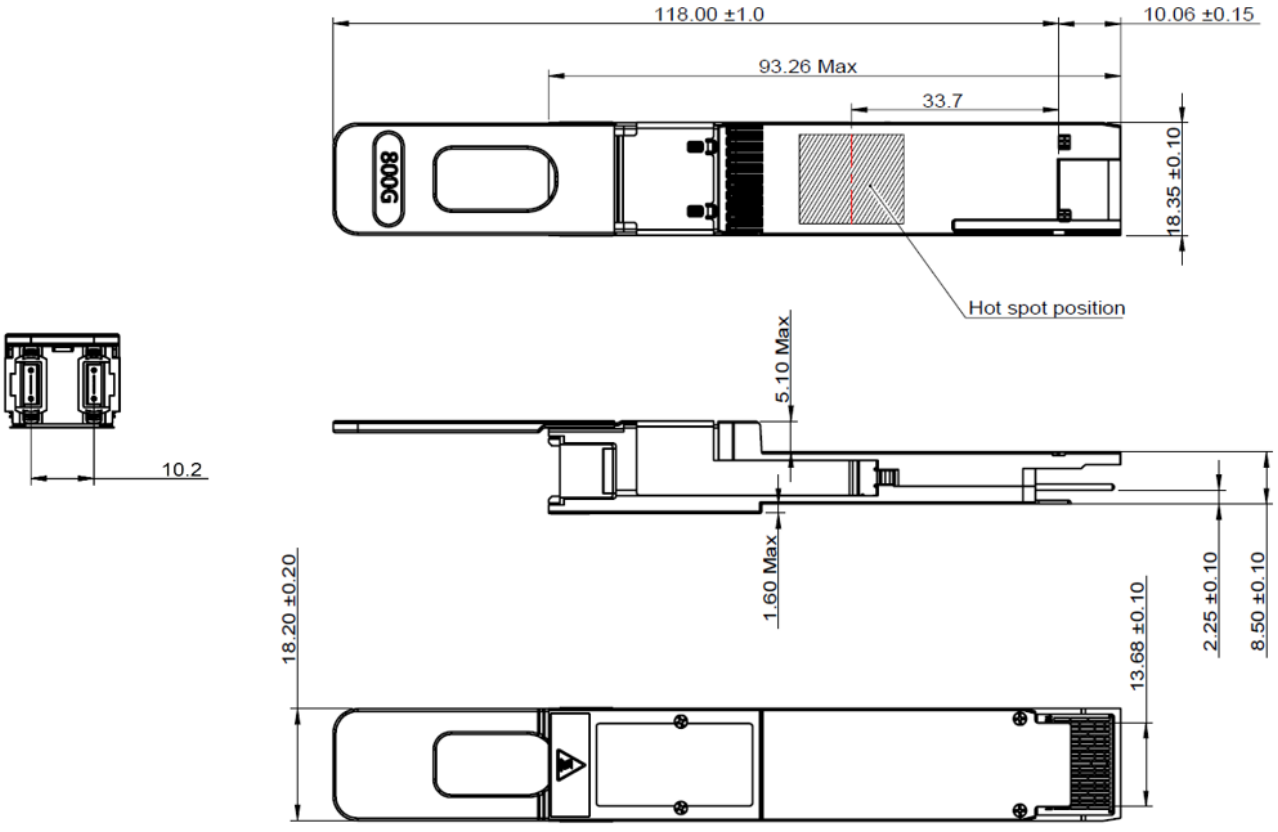

Figure 4 Mechanical Specifications (mm)

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	ºC	
Operating Case Temperature	T_{OP}	0	70	ºC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	PAM4
Link Distance	D			500	m	[1]

Note:

1. FEC required on host system to support maximum distance.

PIN Description

The electrical interface of QSFP112-DD module consists of 76 contacts edge connectors. It complies with the QSFP-DD MSA Specification.

QSFP112-DD Pin Description

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND	Ground			1B
2	TX2n	Transmitter Inverted Data Input	CML-I	Input from Host	3B
3	TX2p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3B
4	GND	Ground			1B
5	TX4n	Transmitter Inverted Data Input	CML-I	Input from Host	3B
6	TX4p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3B

7	GND	Ground			1B
8	ModSelL	Module Select	LVTTL-I	Input from Host	3B
9	ResetL	Module Reset	LVTTL-I	Input from Host	3B
10	VccRx	+3.3V Power Supply Receiver		Power from Host	2B
11	SCL	TWI serial interface clock	LVCMOS-I/O	Bi-directional	3B
12	SDA	TWI serial interface data	LVCMOS-I/O	Bi-directional	3B
13	GND	Ground			1B
14	Rx3p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3B
15	Rx3n	Receiver Inverted Data Output	CML-O	Output to Host	3B
16	GND	Ground			1B
17	Rx1p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3B
18	Rx1n	Receiver Inverted Data Output	CML-O	Output to Host	3B
19	GND	Ground			1B
20	GND	Ground			1B
21	Rx2n	Receiver Inverted Data Output	CML-O	Output to Host	3B
22	Rx2p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3B
23	GND	Ground			1B
24	Rx4n	Receiver Inverted Data Output	CML-O	Output to Host	3B
25	Rx4p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3B
26	GND	Ground	CML-O		1B
27	ModPrsL	Module Present	LVTTL-O	Output from Module	3B
28	IntL/RxLOS	Interrupt/optional RxLOS	LVTTL-O	Output from Module	3B
29	VccTx	+3.3V Power supply transmitter		Power from Host	2B
30	Vcc1	+3.3V Power supply		Power from Host	2B
31	LPMode/TxDis	Low Power mode/optional Tx Disable	LVTTL-I	Input from Host	3B
32	GND	Ground			1B
33	Tx3p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3B
34	Tx3n	Transmitter Inverted Data Input	CML-I	Input from Host	3B
35	GND	Ground			1B
36	Tx1p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3B
37	Tx1n	Transmitter Inverted Data Input	CML-I	Input from Host	3B

38	GND	Ground			1B
39	GND	Ground			1A
40	Tx6n	Transmitter Inverted Data Input	CML-I	Input from Host	3A
41	Tx6p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3A
42	GND	Ground			1A
43	Tx8n	Transmitter Inverted Data Input	CML-I	Input from Host	3A
44	Tx8p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3A
45	GND	Ground			1A
46	P/VS4	Programmable/Module Vendor Specific 4	LVCMOS/CML-I		3A
47	P/VS1	Programmable/Module Vendor Specific 1	LVCMOS/CML-I		3A
48	VccRx1	3.3V Power Supply			2A
49	P/VS2	Programmable/Module Vendor Specific 2	LVCMOS/CML-O		3A
50	P/VS3	Programmable/Module Vendor Specific 3	LVCMOS/CML-O		3A
51	GND	Ground			1A
52	Rx7p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3A
53	Rx7n	Receiver Inverted Data Output	CML-O	Output to Host	3A
54	GND	Ground			1A
55	Rx5p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3A
56	Rx5n	Receiver Inverted Data Output	CML-O	Output to Host	3A
57	GND	Ground			1A
58	GND	Ground			1A
59	Rx6n	Receiver Inverted Data Output	CML-O	Output to Host	3A
60	Rx6p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3A
61	GND	Ground			1A
62	Rx8n	Receiver Inverted Data Output	CML-O	Output to Host	3A
63	Rx8p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3A
64	GND	Ground			1A

65	NC	No Connect			3A
66	Reserved	For future use			3A
67	VccTx1	3.3V Power Supply		Power from Host	2A
68	Vcc2	3.3V Power Supply		Power from Host	2A
69	ePPS/Clock	1PPS PTP clock or reference clock input	LVCMOS-I		3A
70	GND	Ground			1A
71	Tx7p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3A
72	Tx7n	Transmitter Inverted Data Input	CML-I	Input from Host	3A
73	GND	Ground			1A
74	Tx5p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3A
75	Tx5n	Transmitter Inverted Data Input	CML-I	Input from Host	3A
76	GND	Ground			1A

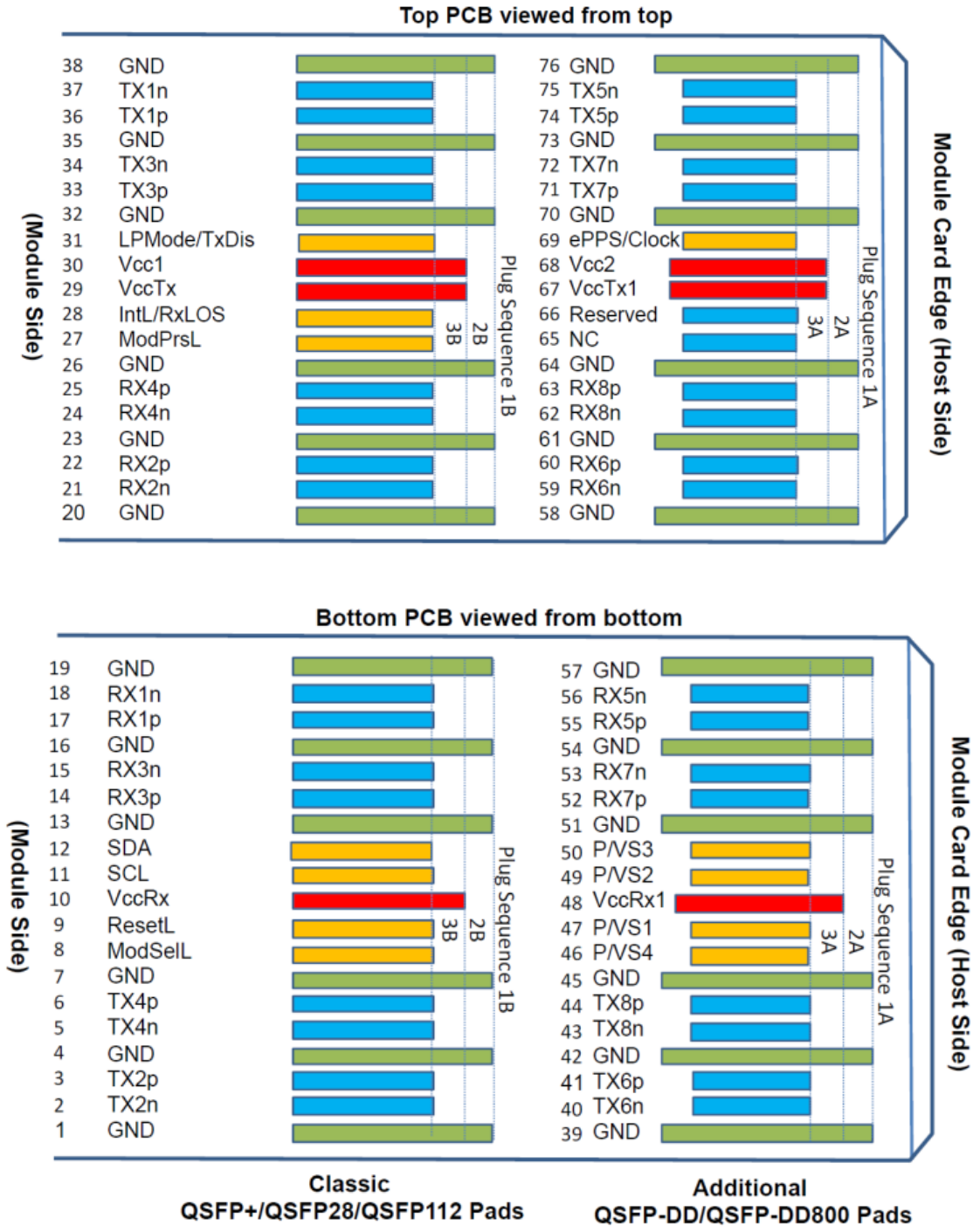

Figure 5 Electrical Pin-out Details

QSFP112-DD Control Signals

Name	Direction	Description
SCL	Bi-Directional	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bi-Directional	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
ModSelL	Input	Input signal that be pulled to Vcc in modules . When held low by host, the module responds to TWI communication commands . When held high by host, the module shall not respond to TWI communication commands.
ResetL	Input	ResetL shall be pulled to Vcc in the module. A low level on it for longer than t_Reset_init initiates a complete module reset.
LPMode/TxDis	Input	Input signal from host with active high logic . Only support behaving as LPMode.
ModPrsL	Output	ModPrsL shall be pulled up to Vcc host and pulled low in the module . When the module is inserted, it's asserted "Low" . When the module is absent, it's deasserted "High".
IntL/RxLOSL	Output	Active-low, open-collector output signal from module . Only support behaving as IntL . When IntL is asserted Low, it indicates a change in module state.

Digital Diagnostic Specification

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	℃	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	[1]
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	[1]

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Regulatory Compliance

Asterfusion OT-800G-QDD-2DR4 transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) EN 60825-1-2014 FDA 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

References

1. QSFP-DD MSA Specification
2. CMIS

ESD

This transceiver is specified as ESD (Electrostatic Discharge) threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 / JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Order Information

Part Number	Description
OT-800G-QDD-2DR4	800G, QSFP-DD, 2DR4, Dual MPO12/APC, 1310nm SMF, 500m/OS2

Warranty and Service Support

Asterfusion optical transceivers come with 2-year Basic H/W service and warranty.

To acquire more info about company, products, and solutions: *www.cloudswit.ch*
Sales: *bd@cloudswit.ch*
Business Hotline: +86-0512-62982976